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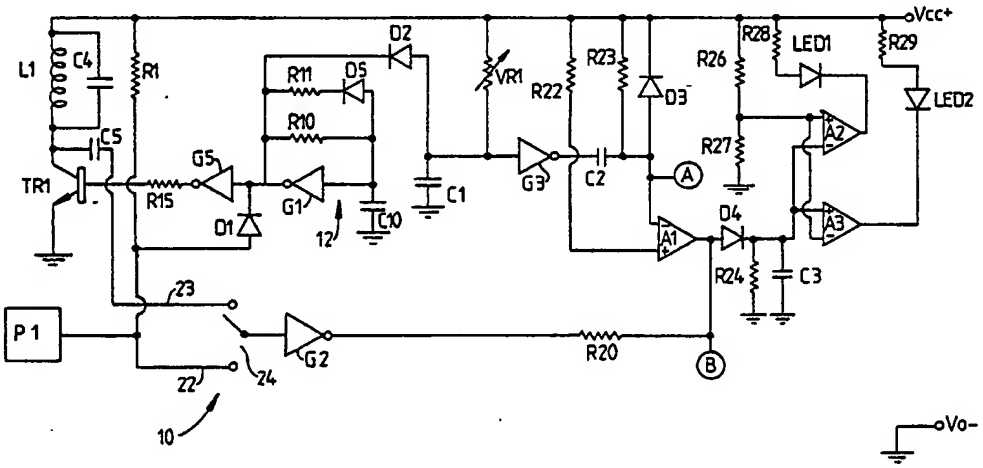
(54) Title: DETECTOR DEVICE



(57) Abstract

A detector device (10) comprising an oscillator (L2) for generating a signal, an inductance (L1) and a metal plate (P1). The signal is applied to these elements whereby to generate respective first and second detection signals respectively influenced by the presence of a metal object in the vicinity of the inductance (L1) and by the presence of a dielectric object in the vicinity of the plate (P1).

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DETECTOR DEVICE

This invention relates to a detector device. In one aspect the invention provides a detector device comprising a generator for generating a signal, a first detector element and a second detector element, means for applying said signal to the first detector element and to the second detector element whereby to generate respective first and second detection signals respectively influenced by the presence of a metal object in the vicinity of the first detector element and by the presence of a dielectric object in the vicinity of the second detector element.

The first detector element is of a kind having its inductance varied in the presence of said metal object, the second detector element being of a kind wherein leakage current therefrom, as produced in use, varies when it is in the vicinity of a dielectric object. The generator means in use generates a pulse which is applied to the first and second detector elements.

The detector device includes means for generating from the signal when applied to the first and second elements an output signal the relative time of occurrence of a particular identifiable feature of which varies when a metal object is brought into the vicinity

of the first detector element and when a dielectric object is brought into the vicinity of the second detector element. The identifiable feature is an edge of a pulse comprised in said output signal. Preferably the detector means comprises means for generating from the output signal an identification signal the magnitude of which is influenced by the relative time of occurrence of said identifiable feature. Preferably, said generator comprises an oscillator generating repetitive input pulses.

The invention is further described by way of example only with reference with the accompanying drawings in which:

Figure 1 is a circuit diagram of a detector device constructed in accordance with the invention;

Figures 2A to 2H inclusive are wave-form diagrams showing various signals present in a detection part of the circuit of Figure 1.

Figures 3A to 3C inclusive are wave-form diagrams illustrating operation of the device of Figure 1 when used for detecting dielectric objects;

Figures 4A to 4C inclusive are wave-form diagrams illustrating operation of the device of Figure 1 when used for detecting metal objects; and

Figure 5 is a diagram showing a modification to the circuit of Figure 1.

The detector device 10 shown includes an oscillator 12 formed from a Schmitt inverter G1 having its input connected to ground via a capacitor C10 and to its output via a resistor R10 and a parallel connected series circuit comprising a resistor R11 and diode D5. The output signal 13 of oscillator 12 is shown in Figure 2A as being in the form of negative going pulses 14,

these being of about 0.5 micro-second duration, at a frequency of about 10 kilohertz.

The signal from the oscillator 12 is applied, on the one hand, via an inverter G5 and series resistor R15, to the base of a transistor TR1 and, via a diode D1, to a metal plate P1.

Plate P1 comprises a detector element for detecting dielectric articles when in the vicinity of the detector device 10. Another detector element, for detecting the presence of metallic objects in the vicinity of the detector device 10 is formed by an inductance L1. Transistor TR1 has its emitter connected to ground and its collector connected to positive supply via the inductance L1. Inductance L1 is connected in parallel with a capacitance C4.

Plate P1 is coupled to positive supply via a resistor R1. Signal from plate P1 is taken therefrom via a line 22 to switch 24. Signal from the collector of transistor TR1 is taken via a capacitor C5 to switch 24, via a line 23. Switch 24 is a double-throw single-pole switch effective, when in one position, to connect line 22 to the input of a Schmitt inverter G2 and, when in the other position, to connect output of transistor TR1 on line 23 to the inverter G2.

The output of inverter G2 is connected via a resistor R20 to the output of a coincidence detector A1. Detector A1 has its non-inverting input connected to positive supply via a resistor R22 and its inverting input connected to positive supply via a diode D3. A resistor R23 is connected in parallel with diode D3. The inverting input is also connected to receive output from oscillator 12 via a series circuit comprising diode D2, Schmitt inverter G3 and capacitor C2. The input of

inverter G3 is connected to ground via a capacitor C1 and to positive supply via a variable resistor VR1.

Output from detector A1 is connected via a diode D4 to the inverting input of a comparator A2 and to the non-inverting input of a comparator A3. These inputs are also connected to ground by a parallel circuit comprised of a resistor R24 and capacitor C3. The remaining inputs of the comparators A2, A3 are commonly connected to a fixed reference voltage circuit comprising two resistors R26, R27 connected in series across the supply, these inputs being connected to the junction between these resistors. Output from comparator A2 is connected to positive supply via a light emitting diode LED1 and series resistor R28 whilst output from comparator A3 is connected to positive supply via the series connected light emitting diode LED2 and resistor R29.

The switch 24 is effective, when operated to connect inverter G2 to line 22, to condition the device 10 for dielectric object detection and, when operated to connect the inverter G2 to line 23, to condition the device 10 for metal object detection.

The operation of the device when switch 24 is operated to condition the apparatus for dielectric object detection is first described:-

Firstly, the output from oscillator 12, comprising the pulses 14 of Figure 2A, is applied via diode D1 to plate P1. Plate P1 is, in the absence of dielectric object in the vicinity thereof and in the absence of application of a pulse from oscillator 12 thereto, raised to a potential of approximately Vcc being the voltage of positive supply applied to the device. This arises because the only ground connection for the plate

P1 is provided by the high input resistance of inverter G2 and by the capacitance presented across the plate P1 to ground, represented principally by the input capacitance of the device G2. In a steady state condition, then, substantially no current flow through resistor R1 occurs. However, on application of a pulse 14 to the plate P1 via diode D1, resistor R1 is effectively grounded for the duration of the pulse whereby the voltage on line 22, as across plate P1, falls to substantially zero. After termination of such pulse however, the potential of line 22 will rise again to the supply voltage Vcc, following an exponentially rising curve the rate of rise being dependant upon the value of resistor R1, the input capacitance of inverter G2 and any losses from plate P1 occurring by current flow through resistor R1 to plate P1 as will occur when a dielectric object is in close proximity to the plate P1. Thus, the rise rate is dependant upon whether or such an object is present in the vicinity of the plate P1. The resultant output signal 15 as applied on line 22 to inverter G2 is shown at figure 2B as comprising negative going pulses 32, the exponentially rising trailing edges of the pulses been shown at 32a.

Inverter G2 will switch, at its output, from a low to a high state as the potential on line 22 rises above a threshold voltage represented at 34 in Figure 2B. Thus, the inverter is switched on at times coinciding with the negative going leading edges of the pulses 32 and off at times when the rising trailing edge 32a of each pulse 32 crosses the threshold 34. The resultant output signal 17 from inverter G2 exhibits a series of a positive going pulses 36 as shown in Figure 2C, where the pulses have a frequency the same as that of the

oscillator 12 but have a pulse width that varies in accordance with the rate of rise of the voltage on plate P1.

Coincidentally with application of the negative going pulses from oscillator 12 to plate P1, these pulses are fed via diode D2 to a pulse stretching circuit comprising the R.C. network of capacitor C1 and variable resistor VR1, together with the Schmitt inverter G3. Capacitor C1 charges via resistor VR1 to approximately Vcc in the absence of negative going pulses 14, which pulses discharge capacitor C1 via diode D2. At the end of each such pulse, capacitor C1 charges via the variable resistor VR1 at an exponentially rising rate so that the input signal 19 presented at inverter G3 exhibits the negative pulses 38 shown in Figure 2D, these having leading edges coincidence with the leading edges of the pulses 14 and trailing edges of exponentially rising form. Inverter G3 is triggered on at the leading edges of the pulses 38 and off when the voltage at the trailing edge of each pulse 38 rises above a threshold value 40 for the inverter G3. Thus, the output 21 of inverter G3 shown at Figure 2E comprises relatively inverted "stretched" pulses 42 corresponding in frequency to the frequency of oscillation of oscillator 12 and having a pulse length dependant upon the value of resistor VR1 which value is variable to permit variation of the pulse length.

The stretched pulse output from inverter G3 is differentiated by capacitor C2 and clipped by diode D3. As shown in Figure 2F, the resultant output signal 23, at the point "A" shown in the circuit, exhibits negative going pulses 44 with a frequency exactly corresponding to that of the oscillator 12 but which pulses are

delayed relative to the leading edges of corresponding pulses 14 by a time pre-settable in accordance with the setting of the resistor VR1.

Detector A1 is effective to bring together the delayed pulses 44 generated at point A and signal derived from the variable width pulses generated at the output of inverter G2, in such a way that any increase of decrease in pulse width caused by losses from plate P1 due to presence of the dielectric object can be determined.

Figure 3A shows, at (a), (b) and (c), three pulses 36 from inverter G2, for respective conditions where the pulse width is at a static condition, where the pulse width is increased, and where that width is decreased.

Detector A1 is in this instance an open collector voltage comparator, and may be considered as being equivalent to a PNP transistor having its collector coupled to the output of inverter G2, its base connected to point "A" and its emitter connected to Vcc. Output will only appear when there is a positive signal present at the output of inverter G2 and a negative voltage at point "A". Thus, only when a pulse 36 overlaps with a pulse 44 will a signal appear at the output of the comparator A1, at the point "B" shown.

Pulses 44 are shown in Figure 3B at (d), (e) and (f). These are illustrated as occurring at respective constant delays after the beginning of corresponding pulses 14 and thus at respective constant delays after beginning of corresponding pulses 36. The actual delay is established by adjusting variable resistor VR1 so that under a predetermined "static" condition of the pulses 36 ((a) in Figure 3A) the trailing edges of pulses 36 barely coincide with the pulses 44. The

result will be an output pulse 60 from comparator A1 as shown at (g) in Figure 3C. This pulse has an amplitude about midway between ground and Vcc. In this regard, it will be noted that the leading edge and, more particularly, the trailing edge of each pulse 36 exhibit some slope while the training edges of pulses 60 also exhibit some slope. Thus, the actual amplitude of the pulses 60 will be influenced by the extent of overlap of pulses 36 and 44, the magnitude being determined by the magnitude of pulses 36, 44 at the times of overlap. Now, when pulses 36 are of greater duration, the magnitudes of pulses 36 and 44 which are reached during overlap will be greater so that with increasing overlap the amplitude of output pulses 60 will increase until at a predetermined degree of overlap a maximum amplitude of somewhat less than Vcc will prevail ((h) in Figure 3C) after which, with increasing overlap, the amplitude will not increase, but the pulse widths of pulses 60 will increase. Conversely, when the output pulses 36 from inverter G2 are of decreased duration, the time of overlap of pulses 36, 44 will decrease so that the magnitude of the output pulses 60 will, as shown at (i) in Figure 3C, decrease. The amplitude of pulses 60 thus indicates the losses occurring from plate P1 and is representative of the presence or absence of a dielectric object in the vicinity of the plate P1, or more particularly is representative changes in thickness of a dielectric material introduced near plate P1. The output pulses from detector A1 are applied via diode D4 to charge capacitor C3 whereby to produce a DC voltage having an amplitude approximately equal to the magnitude of the output pulses 60 from detector A1. The comparators A2, A3 are coupled to illuminate diodes

LED1, and LED2 respectively when the output magnitude from capacitor C3 increases or decreases relative to the fixed voltage level applied to these from voltage divider R26, R27. More particularly, to use the device for detection of dielectric loss variation in materials near plate P1, the resistor VR1 may be adjusted so that neither of diodes LED1, LED2 is illuminated, whereafter, on movement of the detector over the material, one or other of the diodes will be illuminated when such variation is encountered.

The operation of the device 10 in the metal detecting mode is now described.

The negative going pulses generated by oscillator 12 and inverted by inverter G5 are, as described, fed to the base of the NPN transistor TR1. Transmission TR1 is caused to conduct for the duration of each pulse, whereby to cause current flow through the parallel connected inductance L1 and capacitor C4. These comprise a resonant circuit, and after cessation of each pulse, there will be induced into this resonant circuit an exponentially decaying oscillation having an oscillation frequency dependent on the time constant of the circuit comprised of inductance L1 and capacitor C4. Figure 2G shows this exponentially decaying oscillating voltage at 70. This voltage is fed via DC blocking capacitor C5 to the inverter G2. When the amplitude of the decaying oscillating voltage swings above and below the threshold voltage of inverter G2, pulses are produced whereby each oscillating voltage gives rise to a rectangular pulse train 72 at the output of inverter G2 as shown in Figure 2H. This pulse train is formed from a plurality of positive pulses 72a. This pulse train is applied via resistor R2 to the detector A1.

The "delayed pulses" 44 appearing at the point "A" are, by suitable adjustment of resistor VR1, so delayed and that these pulses 44 are brought into coincidence with either leading or trailing edge transitions of chosen pulses 72a of the pulse train 72 from inverter G2. The coincidence detector A1 operates in a fashion somewhat similar to that previously described, in the dielectric detection mode, to produce variable amplitude pulses with changing coincidence between the "delayed pulse" 44 and the chosen pulse of pulse train 72. With greatly increasing coincidence, the pulse width of the resultant output, as before, increases in width once the amplitude approaches voltage Vcc. This action is described more fully later.

In the metal detector mode, the frequency of the exponentially decaying oscillating voltage produced at the collector of transistor TR1 changes as metal is brought into proximity with the inductance L1. The frequency will be reduced when ferrous metal is introduced into the vicinity of the inductance and decreased when non-ferrous metals are so introduced. The manner in which this changing frequency is effective to increase or decrease of the amplitude of the output from detector A1 is illustrated in Figures 4A, 4B and 4C where the voltages at points A and B, together with the form of the output pulse trains 72 at inverter G2 for each applied pulse 14 to transistor TR1 are shown for three conditions, namely a static condition (Figure 4A) where there is no metal adjacent to inductance L1, a condition (Figure 4B) where the frequency of the output train is increased due to introduction of a non-ferrous object and a condition (Figure 4C) where the frequency has decreased with introduction of a ferrous object. In

the static condition of Figure 4A, the timing of pulses 44 at point A is shown as arranged to coincide with the leading edge of the third pulse 72a of each pulse train 72 produced from inverter G2, in such a fashion that the resultant output "B" comprises respective pulses 60 of an intermediate magnitude. Where the frequency of the pulse trains 72 increases as shown in Figure 4B, the relative point of occurrence of the pulses 44 is different and no longer coincides with a leading edge of the forementioned third pulses. Thus, there is an increased coincidence time between the selected pulses 72a and the corresponding pulses 60 so that the resultant output pulses 60 from detector A1 are increased in amplitude. Similarly, when there is a decrease in frequency of the pulse train 72, as in Figure 4C, the amplitude of pulses 60 from detector A1 drops.

To use device 10 in the metal detecting mode, then, variable resistor VR1 is adjusted, in the absence of a metal object, to give pulses 60 of the form shown in Figure 4A, and any increase or decrease in the amplitude as represented by Figures 4B and 4C will be signalled by illumination of diodes LED1, LED2.

The described instruction has been advanced merely by way of explanation and many modifications and variations may be made thereto. For example, while the described arrangement uses a pair of light emitting diodes LED1, and LED2 for detecting increase or decrease in pulse length as applied from inverter G2, other suitable apparatus may be employed such as a suitable meter and associated circuitry to indicate not only the fact of increase or decrease of pulse length, but also to give some indication of the magnitude of such increase or decrease.

A suitable circuit is shown in Figure 5 where, also, the comparator A1 is shown replaced by an NPN transistor TR2. Here, output of inverter G3 is shown coupled via capacitor C2 to the junction of two resistors R50, R51. These are coupled between Vcc and the base of the transistor TR2. The collector of transistor TR2 is coupled to the output of inverter G2, via resistor R20, whilst the base of this transistor TR2 is coupled to ground. Diode D4 couples from the collector of transistor TR2 to the base of a transistor TR3. The collector of transistor TR3 is coupled to Vcc whilst the emitter is connected to ground via the meter M.

Parallel capacitor C3 and resistor R24 couple to the base of transistor TR3 to ground.

Generally, comparator A1 may be replaced by an AND or EXOR gate or any other means suitable for detecting overlap of pulses. Depending on the mode of action of such means, it may be necessary to change the voltage sense at point A, by inversion so that the signal pulses at that point are positive going.

Aside from the above modification, a further modification would be to insert a resistor to present a resistance between resistors R26 and R27 instead of coupling these together. In this case the non-inverting input of comparator A2 is connected to the junction between resistor R26 and the newly inserted resistor, while the inverting input of comparator A3 is connected to the junction between resistor R27 and the newly inserted resistor. This provides that there is a small range of signal magnitudes, as presented to the inverters A2, A3, for which neither LED1, LED2 is illuminated.

Embodiments of the invention are useful as detectors capable of being set to a condition where they are able to detect the presence of wall studs behind the wall (dielectric variation detection) or to a condition where they are able to detect electric wiring within a wall (metal detection).

These and many other modifications may be made without departing from the spirit and scope of the invention which includes every novel feature and combination of novel features as defined in the appended claims.

CLAIMS

1. A detector device comprising a generator for generating a signal, a first detector element and a second detector element, means for applying said signal to the first detector element and to the second detector element whereby to generate respective first and second detection signals respectively influenced by the presence of a metal object in the vicinity of the first detector element and by the presence of a dielectric object in the vicinity of the second detector element.

2. A detector device as claimed in claim 1 wherein the first detector element is of a kind having its inductance varied in the presence of said metal object, the second detector element being of a kind wherein leakage current therefrom, as produced in use, varies when it is in the vicinity of a dielectric object.

3. A detector device as claimed in claim 2 wherein the generator means in use generates a pulse which is applied to the first and second detector elements.

4. A detector device as claimed in claim 3 arranged wherein said pulse is in use applied singularly and selectively to the first and second elements.

5. A detector device as claimed in claim 3 arranged wherein said pulse is in use applied in parallel to the first and second elements.

6. A detector device as claimed in claim 4 or claim 5 wherein the detector device includes means for generating from the signal when applied to the first and second elements an output signal the relative time of occurrence of a particular identifiable feature of which varies when a metal object is brought into the vicinity of the first detector element and when a dielectric object is brought into the vicinity of the second detector element.

7. A detector device as claimed in claim 6 wherein said identifiable feature is an edge of a pulse comprised in said output signal.

8. A detector device as claimed in claim 7 wherein the detector means comprises means for generating from the output signal an identification signal the magnitude of which is influenced by the relative time of occurrence of said identifiable feature.

9. A detector device as claimed in claim 8 wherein said generator comprises an oscillator generating repetitive input pulses.

10. A detector device substantially as hereinbefore described with reference to the accompanying drawings.

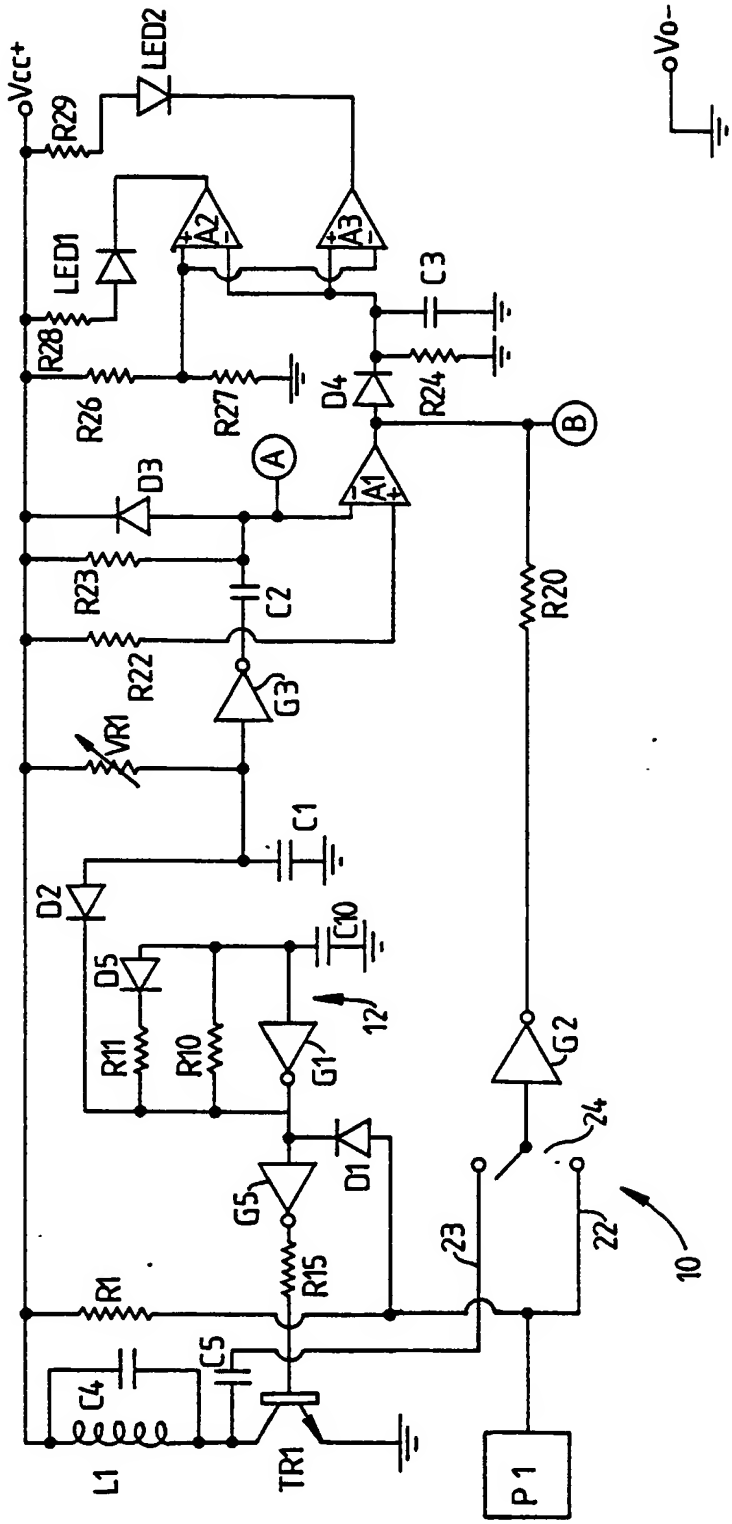
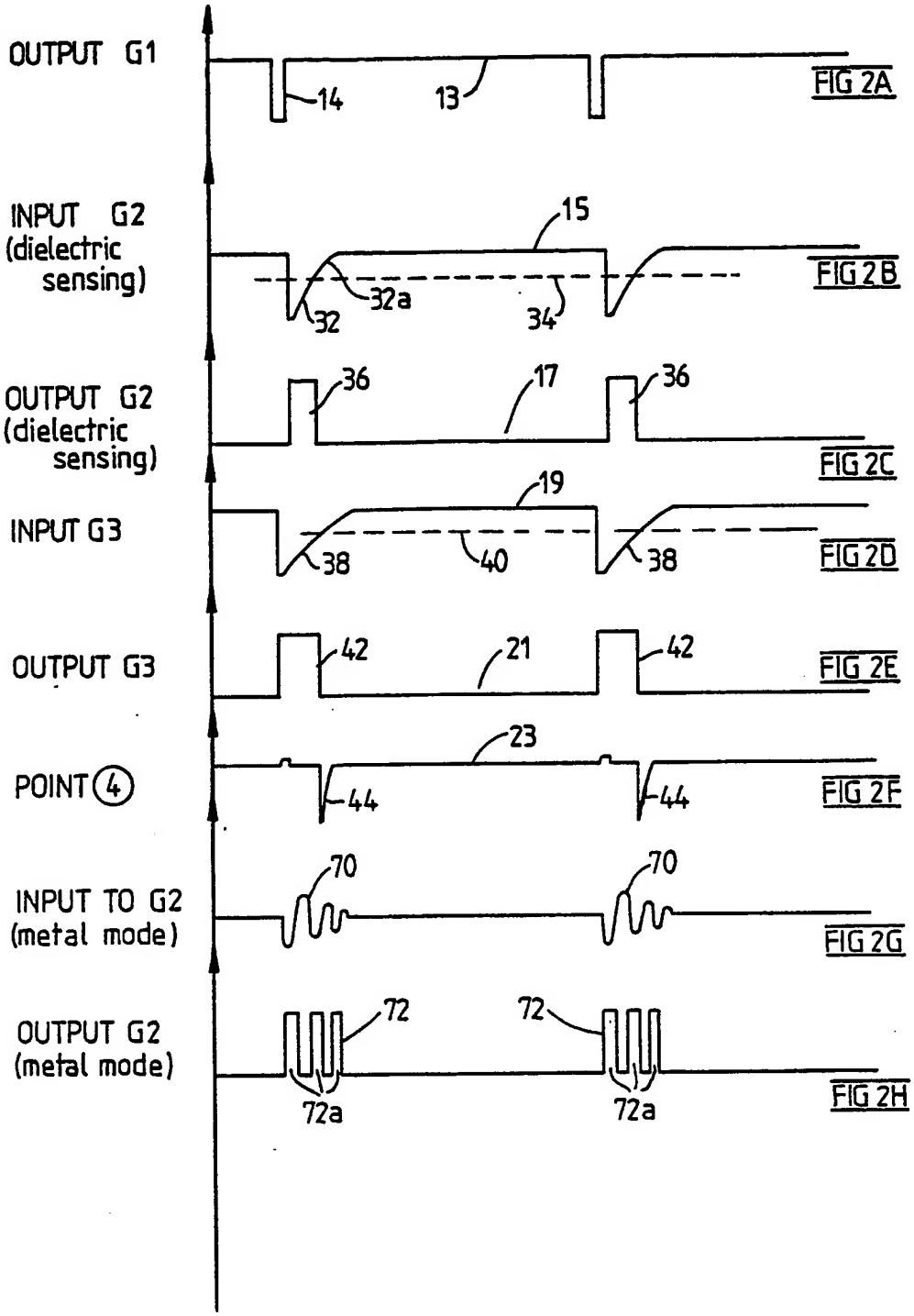
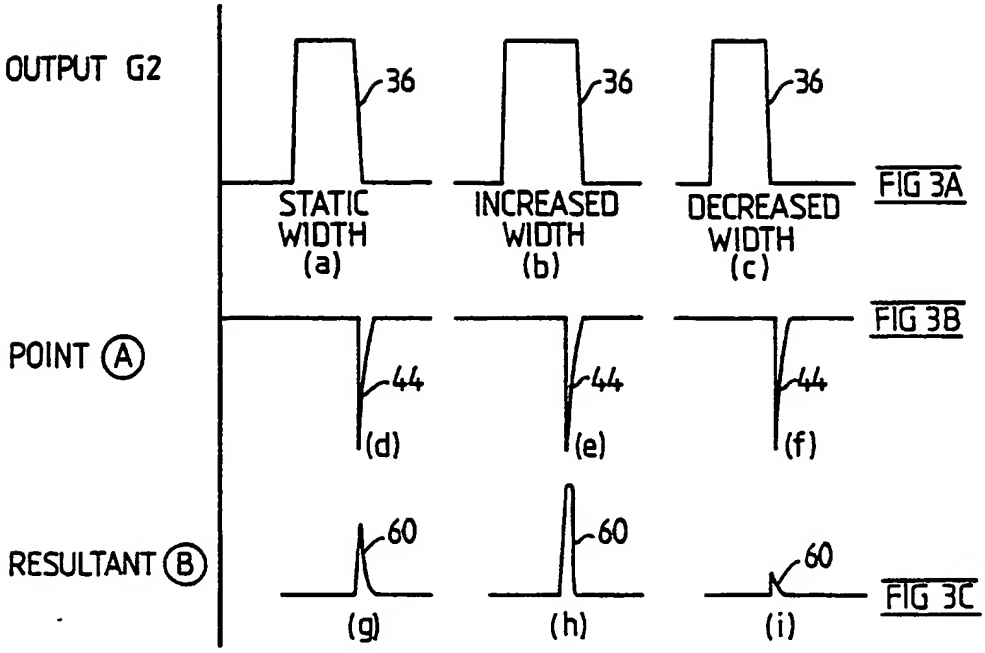
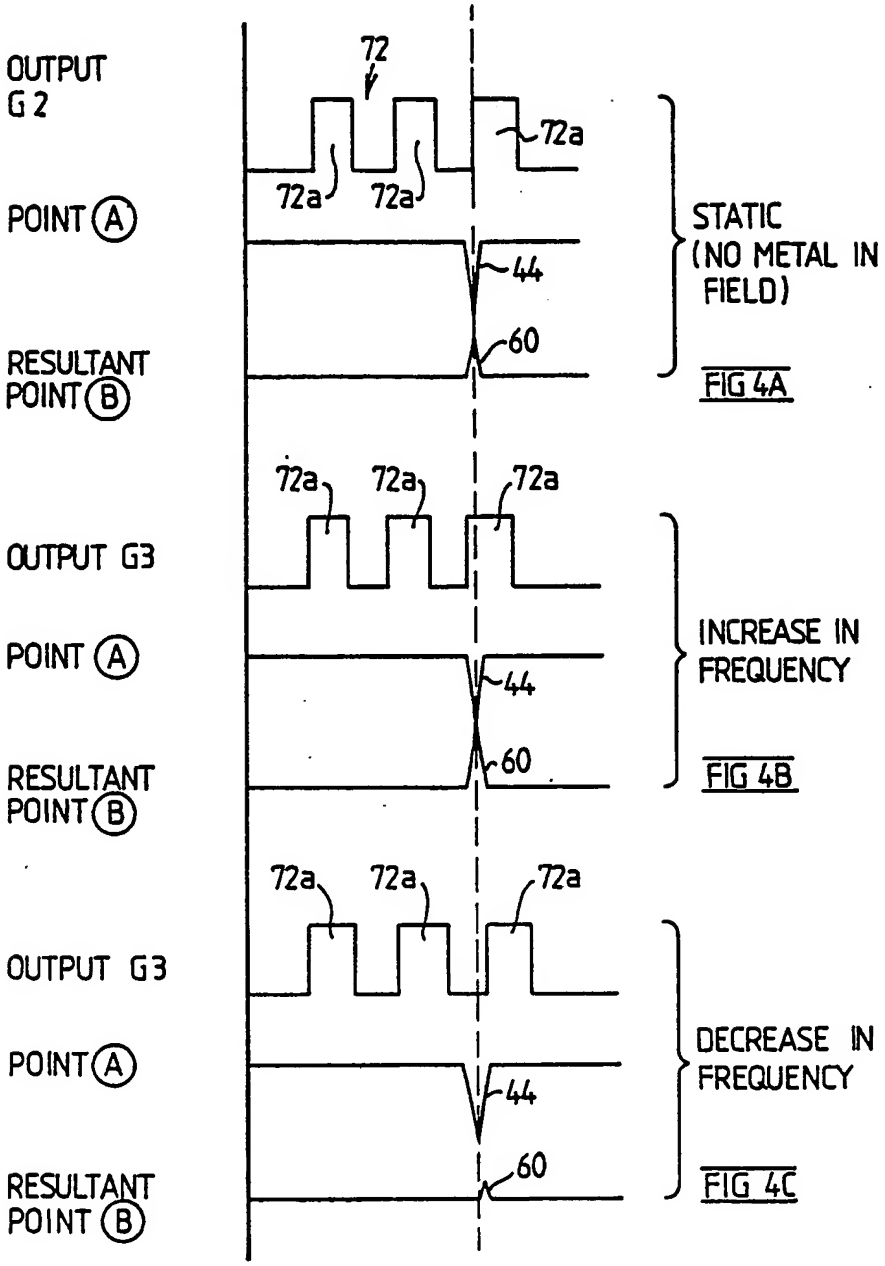

Vcc+
LED2
R29
LED1
R28
R26
R27
A2
A3
C3
D4
R24
B
A
A1
D3
R23
C2
R22
G3
VR1
C1
D2
C10
D5
R11
R10
G1
12
G2
24
D1
G5
R15
23
22
10
R1
C5
C4
L1
TR1
P1
Vo-

FIG 1


OUTPUT G1
14
13
FIG 2A
INPUT G2
(dielectric
sensing)
15
32
32a
34
FIG 2B
OUTPUT G2
(dielectric
sensing)
36
17
36
FIG 2C
INPUT G3
19
38
40
38
FIG 2D
OUTPUT G3
42
21
42
FIG 2E
POINT (4)
23
44
44
FIG 2F
INPUT TO G2
(metal mode)
70
70
FIG 2G
OUTPUT G2
(metal mode)
72
72
72a
72a
FIG 2H


OUTPUT G2
36
36
36
STATIC WIDTH (a)
INCREASED WIDTH (b)
DECREASED WIDTH (c)
FIG 3A
POINT (A)
44
44
44
(d)
(e)
(f)
FIG 3B
RESULTANT (B)
60
60
60
(g)
(h)
(i)
FIG 3C


OUTPUT G2
72
72a
72a
72a
POINT (A)
44
STATIC (NO METAL IN FIELD)
RESULTANT POINT (B)
60
FIG 4A
72a
72a
72a
OUTPUT G3
POINT (A)
44
INCREASE IN FREQUENCY
RESULTANT POINT (B)
60
FIG 4B
72a
72a
72a
OUTPUT G3
POINT (A)
44
DECREASE IN FREQUENCY
RESULTANT POINT (B)
60
FIG 4C

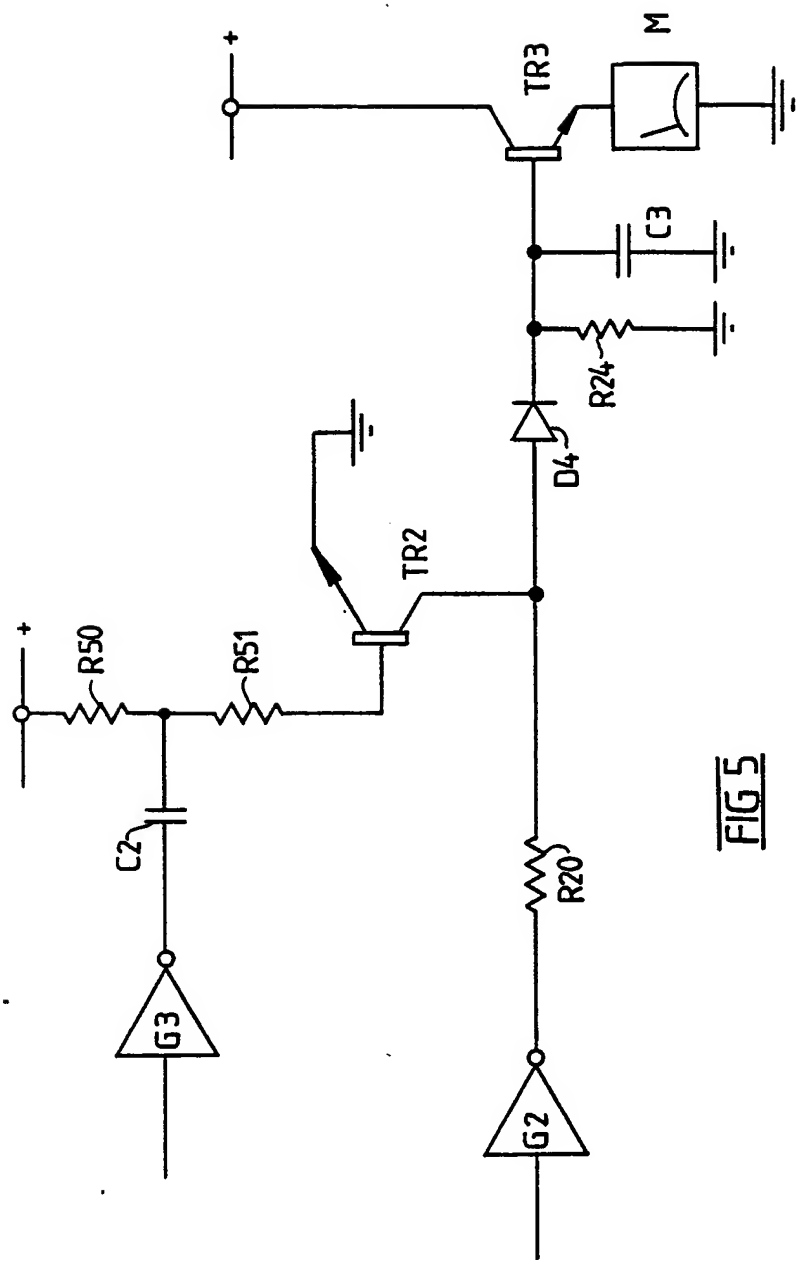


FIG 5

INTERNATIONAL SEARCH REPORT

International Application No PCT/AU 86/00220

I. CLASSIFICATION OF SUBJECT MATTER

According to International Patent Classification (IPC) or to both National Classification and IPC

Int. Cl.[4] G01V 3/10

II FIELDS SEARCHED

Minimum Documentation Searched

Classification System	Classification Symbols
IPC	G01V 3/08, 3/10, 3/11

Documentation Searched other than Minimum Documentation to the Extent that such Documents are Included in the Fields Searched

AU : IPC as above

III DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of Document, with indication, where appropriate, of the relevant passages	Relevant to Claim No
X	GB,A, 2146128 (GORING KERR PLC (UNITED KINGDOM)) 11 April 1985 (11.04.85)	1-6
X	AU,A, 12319/83 (ZIRCON INTERNATIONAL INC.) 15 September 1983 (15.09.83)	1
Y	AU,B, 57702/65 (282113) (SHELL MAATSCHAPPIJ N.V.) 20 October 1966 (20.10.66)	1-2
Y	US,A, 4130793 (BRIDGES et al) 19 December 1978 (19.12.78)	1-2
A	WO,A, 85/02268 (CONSOLIDATED TECHNOLOGY (AUST) PTY LTD 23 May 1985 (23.05.85)	
A	LAGAL, R. et al "VLF-IR Metal Detector Handbook", published 1979, Ram Books (USA) See pages 9-36	

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IV CERTIFICATION

Date of the Actual Completion of the International Search	Date of Mailing of this International Search Report
12 November 1986 (12.11.86)	(25.11.86) 25 NOVEMBER 1986
International Searching Authority	Signature of Authorized Officer
Australian Patent Office	D. HERALD

Form PCT/ISA/210 (second sheet) (January 1985)

ANNEX TO THE INTERNATIONAL SEARCH REPORT ON
INTERNATIONAL APPLICATION NO. PCT/AU 86/00220

This Annex lists the known "A" publication level patent family members relating to the patent documents cited in the above-mentioned international search report. The Australian Patent Office is in no way liable for these particulars which are merely given for the purpose of information.

Patent Document Cited in Search Report	Patent Family Members		
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AU 57702/65	NL 6404386		
AU 12319/83	GB 8306600 JP 58171690	GB 2117909 US 4464622	GB 2159630 GB 8514596
WO 8502268	AU 36178/84 GB 2160661	EP 165256	GB 8515989
US 4130793	CA 1080802		

END OF ANNEX